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BSCpE 3A

**BCD Up Counter**

**VHDL Code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity bcdupcount is

Port ( clk,rst : in STD\_LOGIC;

q : inout STD\_LOGIC\_VECTOR (3 downto 0));

end bcdupcount;

architecture Behavioral of bcdupcount is

signal div:std\_logic\_vector(22 downto 0);

signal clkd:std\_logic;

begin

process(clkd)

begin

if rising\_edge(clk)then

div<= div+1;

end if;

end process;

clkd<=div(22);

process(clkd,rst)

begin

if rst='0' or q="1010" then

q<="1111";

elsif clkd'event and clkd='1' then

q<=q+1;

end if;

end process;

q<=q;

end Behavioral;